	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	(asynchronous with signal) and (circuit with (clock or clocked) with vhdl) and (synchronization with module with iff)	USPAT; EPO; JPO; DERWENT	2004/08/13 09:38
2	BRS	L2	128	(asynchronous with signal) and (circuit with (clock or clocked)) and (synchronization with module)	USPAT; EPO; JPO; DERWENT	2004/08/13 09:48
3	BRS	L3	0	((simulation or simulating) with clock with circuit).ti,ab. and (asynchronous with signals) and vhdl and iff	USPAT; EPO; JPO; DERWENT	2004/08/13 09:51
4	BRS	L4	3	((simulation or simulating) with clock with circuit).ti,ab. and (asynchronous with signals)	USPAT; EPO; JPO; DERWENT	2004/08/13 09:56
5	BRS	L5	41	((simulation or simulating) with clock with circuit) and (asynchronous with signals)	USPAT; EPO; JPO; DERWENT	2004/08/13 10:07
6	BRS	L6	4	(simulate or simulation) adj clock adj circuit	USPAT; EPO; JPO; DERWENT	2004/08/13 10:09
7	BRS	L7	80	(simulate or simulation) same (clock adj circuit)	USPAT; EPO; JPO; DERWENT	2004/08/13 10:10
8	BRS	L8	138	simulate with clock with circuit	USPAT	2004/08/13 10:50
9	BRS	L9	13	(simulate with clock with signal) and (asynchronous with signal) and (synchronous or synchronize or synchronizing)	USPAT; EPO; JPO; DERWENT	2004/08/13 10:54